(19) World Intellectual Property Organization International Bureau





(43) International Publication Date 16 August 2007 (16.08.2007)

(10) International Publication Number WO 2007/090315 A1

- (51) International Patent Classification: H03F 3/00 (2006.01)
- (21) International Application Number:

PCT/CN2006/000210

- (22) International Filing Date: 9 February 2006 (09.02.2006)
- (25) Filing Language:

English

(26) Publication Language:

English

- (71) Applicant (for all designated States except US): APEX-ONE MICROELECTRONICS INC. [GB/CN]; Building 18, No.115 Lane 572 Bibo Road, Zhangjiang Hi-Tech park, Shanghai 201203 (CN).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): ZHU, Hao [CN/CN]; Dan Ying Village, Huang Wan Town, Ling Bi County, Anhui (CN). HUANG, Halbin [CN/CN]; Room 301, No.117, Lao Shan Xin Cun, Xi Xia Road, Shanghai (CN). REN, Yongqing [CN/CN]; Room 201, No.11, Lane 500, Hua Mu Road, Pudong District, Shanghai (CN).

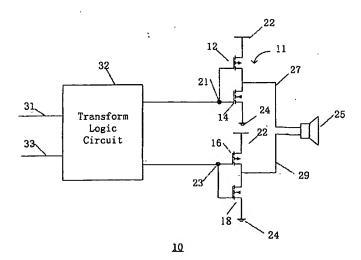
- (74) Agent: SAMSON, G., Yu; Kangxin Partners, P.C., Floor 16, Tower A, InDo Building, A48 Zhichun Road, Haidian District, Beijing 100098 (CN).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

with international search report

[Continued on next page]

(54) Title: SIGNAL MODULATION SCHEME IN CLASS-D AMPLIFICATION AND CIRCUIT THEREFOR



(57) Abstract: A class-D amplifier (10) includes a logic circuit (40) for controlling the operation of a switching bridge (11). The logic circuit (40) transmits the differential mode of a differential pulse width modulation input signal and deletes a central portion of the common mode of input signal, while preserving pulses of a minimum pulse width following a rising edge and preceding a falling edge in common mode of the input signal. Deleting the central portion of the common mode signal improves the efficiency and reduces the electromagnetic interference radiation of the class-D amplifier (10). Preserving the pulses of the minimum pulse width ensures the proper operation of the switching elements (12, 14, 16, 18) in the switching bridge (11), thereby reducing the distortion in the signal amplification.

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.